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OPTIMIZING CONVERTER DESIGN AND PERFORMANCE UTILIZING MICRO CONTROLLER SYSTEM FEEDBACK AND CONTROL

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Abstract

This paper presents a description of a switching converter design based on a digital philosophy which incorporates proportional and derivative feedback controls to regulate the output voltage. Converter design and performance is optimized by using offset and scaling in the "analog" feedback loop and includes a balance control and "feedforward or anticipatory" pulse width modulation scheme. The novel features, such as system protection and fault isolation diagnostic functions, along with hardware implementation, are discussed and outlined. The performance results of the hardware implementation are also presented at the end of this paper.

1.0 INTRODUCTION

Traditionally, off-line analog switching regulator designs have resulted in a high component count which adversely affects reliability, package size and overall cost. Analog feedback control systems experience both short and long term stability problems because of component drift. Secondly, each output voltage to be regulated requires a dedicated analog control system. This means that power systems which produce multiple, independent, regulated output voltages must have an independent analog controller for each voltage since many contemporary applications require three to five independent voltages, duplicated analog circuitry contributes significantly to the cost of their power systems. Analog designs are not flexible enough to adapt to widely varying applications.

An ideal feedback control system would be one that could incorporate the advantages of proportional and derivative control for multiple, independent, regulated output voltages at low cost in a simple implementation that is relatively independent of component drift and would adapt to different needs. A feedback control system with all these properties can be achieved by using a digital control philosophy instead of an analog one. All the digital functions could be incorporated into a single LSI circuit chip and produce them economically in a small package size. The digital power system controller (DPSC) provides easy manipulation of numerical reference values and control parameters. This makes a single circuit adaptable to widely varying applications providing a great deal of flexibility.

1.1 OBJECTIVES AND FEATURES

The objectives of the DPSC concept are three fold: (1) to provide the pulse width modulation control for the power supply regulation, (2) to provide system protection and, (3) to provide fault isolation (diagnostic) capability in the event of power supply failure.

A switching regulator which uses digital logic as

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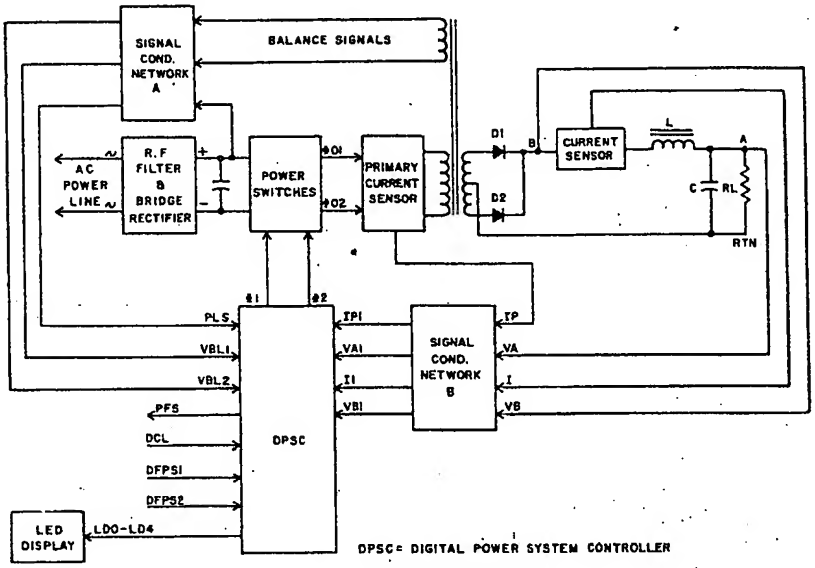


FIGURE 1
COMPLETE DIGITAL POWER SYSTEM

its building blocks to provide proportional/derivative control for minimization of static and dynamic load changes on regulated level and an "anticipatory or feedforward" control for minimization of static and dynamic line changes is outlined. In addition, the digital controller provides the following features:

(1) Frequency programmability up to and beyond 80 kHz to cover bipolar and MOS transistor technologies

(2). Programmable duty cycle limiters for safe operation of a power supply in case of single or double ended rectification schemes.

(3) Drive phase balance control to eliminate the need for a line coupling capacitor in half bridge configurations

(4) Sequencing control of a power system (including power line sense logic)

(5) Remote voltage margin control for field adjustment and evaluating equipment performance

(6) Fault identification diagnostics.

GLOSSARY OF TERMS

Φ 1 and Φ2: These are two duty ratio drive signals that control the output of the power switches.

PFS: This is the "power fail sense" signal, used to initiate an orderly shut down of the system, being driven by the digital power system.

LD0-LD4: The outputs that provide coded fault isolation data to the LED's for display.

V_{A1}: This is a dc level proportional to the regulated voltage at A.

I1: Voltage level proportional to the current at I.

V_{B1}: These are voltage pulses proportional to those at B.

V_{BL1} and V_{BL2}: These are balance signals used to maintain a long term volt-second differential between Φ01 and Φ02 approaching 0 in order to limit the transformer magnetizing current.

PLS: This is a "power loss sense" signal. It senses when the bulk voltage rises above or falls below a certain level of its "on" value reference point. When a rising transition is detected,

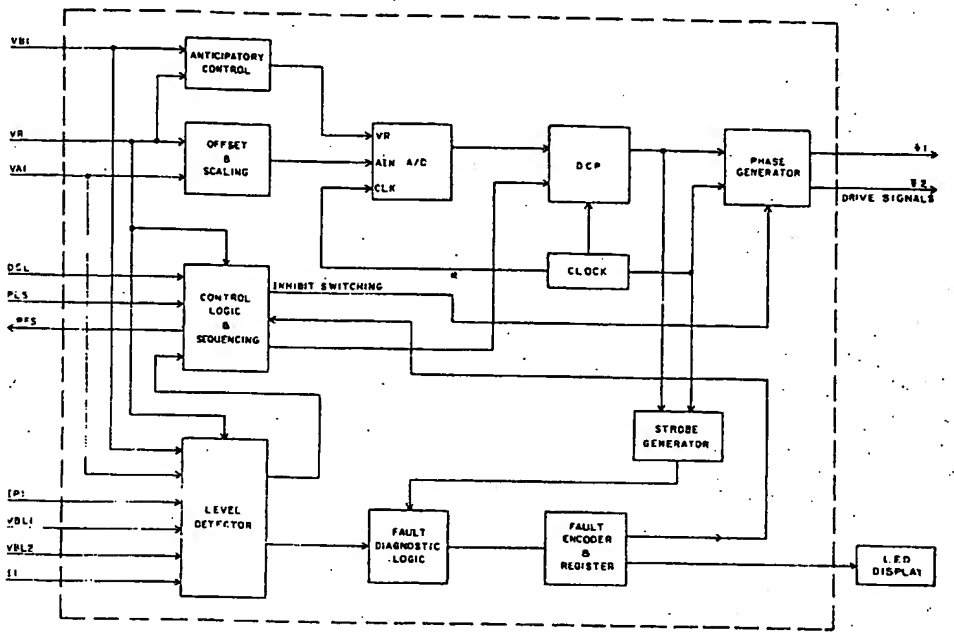


FIGURE 2
FUNCTIONAL BLOCK DIAGRAM OF DPSC

DPSC is initialized and the power up sequence initiated. When a falling transition is detected, PFS signal is activated.

DCL: Programming pin to indicate double ended or single ended rectification scheme.

DFPS1-DFPS2 (Digital Frequency Programmability Signals): Selection of switching frequency will be made according to levels presented on these pins.

IP1: Voltage level proportional to the current in the primary winding of the transformer.

2.0 FUNCTIONAL DESCRIPTION OF DIGITAL POWER SYSTEM CONTROLLER

To illustrate the overall functionability of the DPSC concept within a typical off-line switching regulator, the reader is referred to the block diagram schematics presented in Figures 1 thru 3. In the Figure 1 diagram, the blocks named "DPSC" and "Signal conditioning network" provide the heart of control of the switching power system. The DPSC block contains all the necessary controls of the sequencing, regulation, system protection, and fault protection diagnostic parameters of the system. The primary function of the signal conditioning network is to provide the necessary interface to the controller through passive scaling elements such that the system can be tailored to specific requirements but still maintain a "universal" DPSC design objective.

2.1 DESCRIPTION OF REGULATION FUNCTION (Refer to Figures 2 and 3)

For any digital power system controller to function, the primary requirement is to convert the analog signal, which is the output voltage to be regulated, into a digital number for processing to determine the correction needed. This conversion is accomplished by an A/D converter. The digital proportional and derivative feedback control terms are calculated by the digital control processor (DCP). Sum of the feedback control terms (referred to as the correction term) is added to a reference digital quantity corresponding to a nominal pulse width for a given supply. It is further modified by the DCP as a result of balance control signals to correct for the long term imbalance in the inverter transformer,

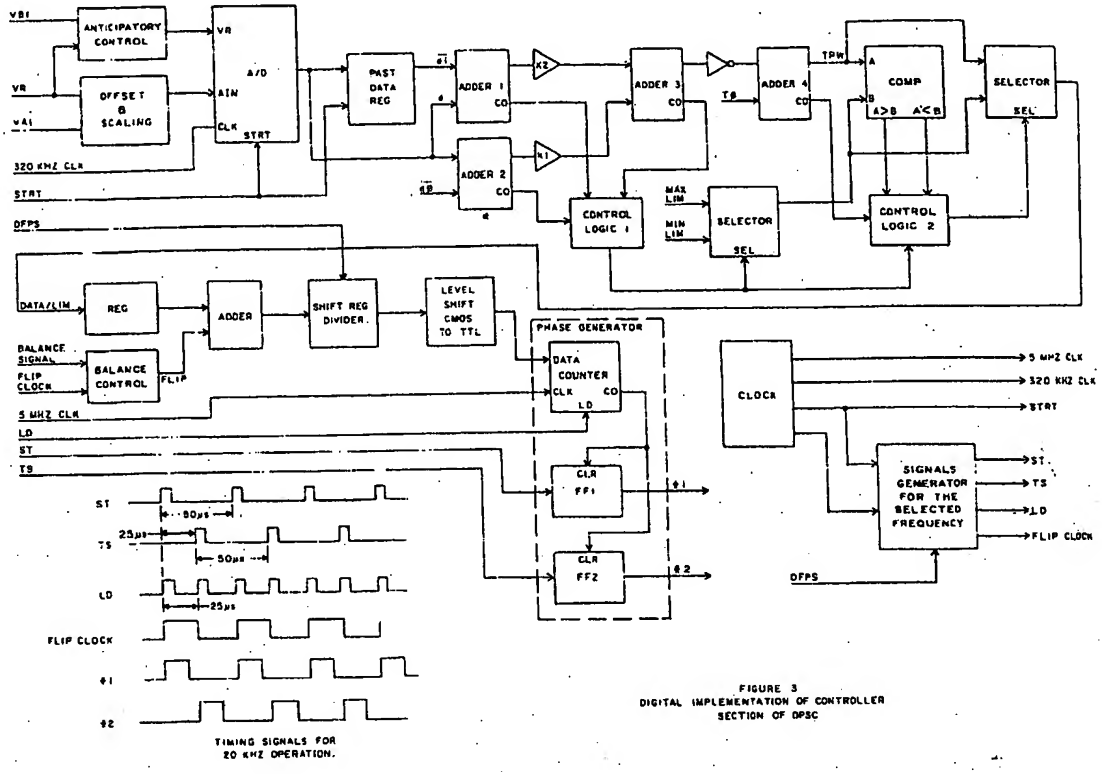


FIGURE 3
DIGITAL IMPLEMENTATION OF CONTROLLER SECTION OF DPSC

resulting in a build up of magnetizing current due to unequal volt-sec drive from the switching transistors. This final digital number is translated into duty ratio drive signals Φ 1 and Φ 2 by the phase generator.

The pulse width is set by sampling the regulated output voltage on a periodic basis and the updating of the pulse width through the calculation process. (Note: In the hardware implementation of the DPSC concept, the sampling rate was set at 20 kHz due to A/D and processor cost/performance tradeoffs.)

By monitoring the power supply output voltage, the DPSC can adjust the duty ratio of the drive signals up or down in small discrete steps to counteract the change in the output voltage. The control equation used in this scheme is given as follows. (Refer to Figure 1.)

$$TPW = TA + TCR$$

where TPW = calculated pulse width

TA = nominal pulse width which determines the static output of the given switching power supply

and TCR = pulse width correction

Nominal pulse width, TA, can be calculated by:

$$V_{Anom} \approx V_{Bnom} \times \frac{TA}{T}$$

which gives $$TA = \frac{V_{Anom}}{V_{Bnom}} \times T$$

where V_{Anom} = nominal output

V_{Bnom} = nominal amplitude of voltage at the input of the power filter. (Includes diode and inductor IR losses)

T = switching period

For a 5 V power supply with 12 V input and 40 kHz switching frequency (measured at point B),

nominal pulse width, TA = 5/12 x 25 us = 10.415 us.

With a 5 MHz clock to the phase generator (a counter and a pair of flip flops which converts numbers into duty ratio; refer to phase generator block of Figure 3), this translates into the decimal number 52 for digital processing.

The pulse width correction, TCR, is calculated by: TCR = -K1(d-d0) -K2(d-d1), where the first term on the right (proportional) feedback control) is to reduce static error and the second term (derivative feedback control) to improve the dynamic response.

d0 = digital equivalent of the nominal output voltage (regulated)

d = digital equivalent of the current (present) sample of the output voltage at A

and d1 = digital equivalent of the preceding sample of the output voltage, VA.

K1 and K2 are digital gain factors. The digital derivative function is approximated by

$$\frac{dVA}{dt} = \frac{(d-d1)}{Ts},$$

where Ts is the sampling period. Ts is absorbed in K2 giving the final form for TCR as shown above.

Changes in the amplitude of the voltage at B are proportional to changes in the amplitude of the power line voltage. Utilization of B, in addition to A, as the duty cycle manipulative information results in an anticipatory or feedforward pulse width modulation scheme resulting in tighter line and load regulation.

How is this accomplished and optimized? Before introducing the analog signal (output voltage) into the A/D converter, it is offset and scaled. The principal relationship between the analog variable and the digital number is proportionality, the repertoire of codes corresponding to a given resolution may represent any portion of the analog voltage or current range. For example, if one wishes to encode the voltage range from 4 to 7 volts in binary, using a 0 - 10 V A/D converter, one could simply apply the voltage without any transformation using only 0.3 of the available number of bits. However, a more efficient alternative would be to offset the input by 4 volts, amplify by 3.33, and apply the resulting 0 - 10 V signal to the converter, thereby making use of the entire range of available codes and improving resolution by a factor of 3. The range of output voltage which is of importance to us is about 4.125 to 5.5 V for a 5 V supply.

2.1.1 Anticipatory Control for Line Regulation

The method of feedforward control is to change the reference voltage VR to the A/D converter according to the line voltage changes, thereby moving the digital codes up or down to counteract the changes in line voltage. Let us review the input/output relationship for the switching power supply:

$$V_A = V_B \times \frac{Ton}{T},$$

where Ton is the ON time and T is the switching period measured at the point, B. This gives

$$Ton = \frac{VA}{VB} \times T$$

with T = 25 us (i.e., fs = 40 kHz) and 5 MHz (0.2 us period) clock to the phase generator, T could be transformed into a decimal number, 25/.02 = 125.

Now we can write our pulse width equation in the form given below considering only the proportional term.

$$\frac{VA}{VB} \times 125 = PWnom - K1(d-d0),$$

where PWnom = nominal pulse width.

$$d = \frac{\frac{VA}{VB} \times 125 - PWnom}{-K1} + d0$$

$$d = \frac{\frac{VAnom}{VBnom} \times 125 - \frac{VA}{VB} \times 125}{K1} + d0$$

Using offset and scaling for the analog input in the form:

$$Ain = 4(VA - 3/4\ VR)$$

where Ain is the offset and scaled analog input and VR is the reference voltage to A/D converter.

$$Ain(nom) = 4(Anom - 3/4\ VRnom)$$

For an A/D with 8 bit resolution, d becomes

$$d = \frac{\frac{VAnom}{VBnom} \times .125 - \frac{VA}{VB} \times 125}{K1} + \frac{4(VAnom - 3/4\ VRnom)}{VRnom} \times 256$$

But

$$d = \frac{4(VA - 3/4\ VR)}{VR} \times 256$$

$$= 1024\ \frac{VA}{VR} - 768$$

$$1024\ \frac{VA}{VR} - 768 = \frac{\frac{VAnom}{VBnom} \times 125 - \frac{VA}{VB} \times 125}{K1} + \frac{4(VAnom - 3/4\ VRnom)}{VRnom} \times 256$$

For the example case, take

VAnom = 5 V, nominal output voltage
VBnom = 12 V
VRnom = 5.5 V

and K1 = 2

We get

$$\frac{VA}{VR} + 0.061\ \frac{VA}{VB} = 0.9346$$

Our aim is to find the relationship between VB and VR which will give a constant output (i.e., VA = 5 V).

$$VR = \frac{1}{0.1869 - 0.061 \times 1/VB}$$

This is the nonlinear relationship between VR and VB and difficult to implement.

Let up plot the curve between VR and VB (Figure 4) to see how it looks in the vicinity of the normal operating point, VR = 5.5 V and VB = 12 V. We will allow +10% variation in the line voltage which is enough for the power supply.

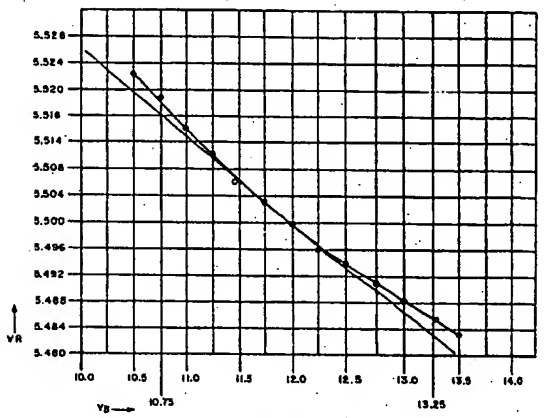


FIGURE 4
VREF VB VR
FEEDFORWARD CONTROL

The plotted curve is linear in the range of 11.25 to 12.5 volts of VB and beyond that the nonlinearity increases. Let us consider the range of VB from 10.75 to 13.25 volts.

VB	VR	ΔVR = VRnom ~ VR	ΔVR (AV) Average	ΔVB = VBnom ~ VB
10.75 V	5.5179 V	0.0179 V		
12.0 V	5.5 V	0.012 V	0.01495V	1.25 V
13.25 V	5.488 V			

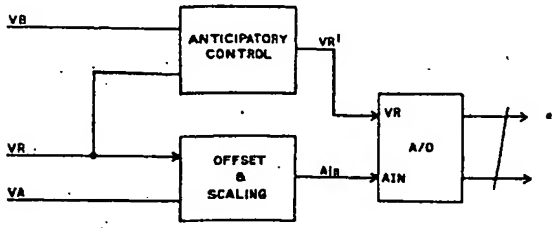
$$\frac{\Delta VB}{\Delta VR} = \frac{1.25}{.01495} = 83.61$$

For normal operating point at VR = 5.5 V and VB = 12 V, the new reference voltage

$$VR' = 5.5 - \frac{\Delta VB}{83.61} = 5.5 - \frac{VB - 12}{83.61}$$

$$VR' = 5.64 - \frac{VB}{83.61}$$

This is the linear equation and can be easily implemented to give the anticipatory control for line regulation. (See below.)

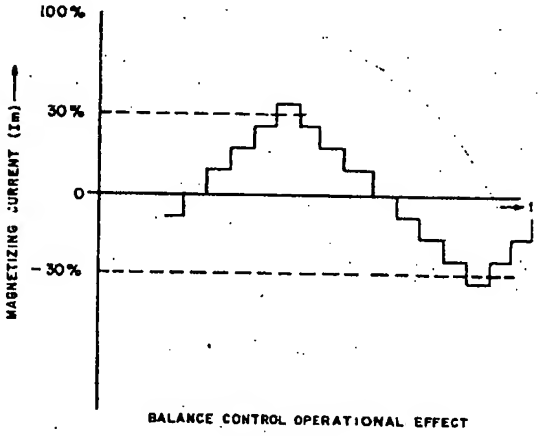


A similar relationship between VA, VB and Ain could be found. Line voltage changes are compensated for by modifying Ain accordingly and keeping the reference voltage VR fixed.

2.2 DESCRIPTION OF BALANCE CONTROL

The use of balance signals is being specified to correct for a long term imbalance in the inverter transformer, resulting in a build up of magnetizing current due to unequal volt-second drive from the power switches.

The effect of balance control operation on magnetizing current (Im) is illustrated in the following figure. A difference of X% in duty cycles of drive signals as a result of balance control operation is introduced, which represents a volt-second imbalance greater than normally expected in the drive electronics. This is done so that the slope of change in magnetizing current, Im, is as independent of the drive electronics as possible. An Im threshold, ±30% of Im (max), is selected which is well below the necessary level of saturation. The DPSC provides a positive and negative threshold detector such that the output is toggled upon the detection of each threshold of opposite sign. When the build up of Im reaches this threshold, the balance comparator (threshold detector) toggles and the DPSC substracts a duty cycle of X/2% from the drive signal which makes the comparator toggle and adds a duty cycle of X/2% to the other drive signal, thus creating a difference of X% in the duty cycle of the drive signals. This forces the Im curve to "walk down", as illustrated in the following figure, until the opposite threshold is reached, where the process is reversed by substracting a duty cycle of X/2% from the drive signal which made the opposite threshold to reach and adds a duty cycle of X/2% to the other drive signal causing a "walk up" and the process is repeated.



BALANCE CONTROL OPERATIONAL EFFECT

Figure 5

2.3 REGULATION SYSTEM OPERATION - BREADBOARD IMPLEMENTATION

A simplified diagram of the regulator section of the digital power system controller is shown in Figure 3. At the falling edge of the STRT signal to the A/D converter, the analog to digital conversion process starts and is complete in about 30 us (limitation of a MOS ADC). The analog signal is sampled every 50 us. The function of the rest of the circuitry is to (a) calculate $TPW = TA - [k1(d-d0) + K2(d-d1)]$, (b) modify this according to the balance control signals and then, (c) to transform this into duty ratio drive signals Φ1 and Φ2. The past data register stores the preceding (past) digital data in the 1's complement form. Adder 1 performs (d-d1) and Adder 2 performs (d-d0), both 2's complement substraction. These terms are multiplied by digital gain factors K1 and K2, respectively. The multiplication becomes easier and simpler, especially when K1 and K2 are integer powers of 2. The operation of shifting a digital number n positions to the

left corresponds to multiplying it by 2^n. Shifting a digital number n positions to the right corresponds to multiplying it by 2^{-n}. This could be achieved by using shift registers performing shift operations as desired or through hard wire strappings. The Adder 3 sums these terms together producing K1(d-d0) + K2(d-d1). This sum could be positive or negative. It is in 2's complement form if negative and in true data form if positive. Adder 4 performs the operation TA + [-T3] giving TPW. Where TA is the hard wired digital number corresponding to nominal pulse width for the given supply. According to the sign of [-T3], the control logic 1 selects the maximum or minimum limit which is set to 9% and 41% duty ratio. This is compared with TPW. Control logic 2 selects the TPW data or appropriate limit as a result of comparison. If the TPW data is greater than the maximum limit, then the maximum limit is selected. If it is less than the minimum limit, then the minimum limit is selected. Otherwise, the TPW data is selected. This data or limit is stored in a register. This data is further modified by the balance control signal and the flip clock. It adds 4% of duty ratio to data corresponding to one phase and substracts 4% from the other phase (Φ 1 and Φ 2) or vice versa, depending on the state of flip signal. The counter and flip flops convert this final digital number into a duty ratio (drive signals Φ 1 and Φ 2).

2.4 DIAGNOSTICS AND SYSTEM PROTECTION PHILOSOPHY

Present analog methods and power system architectures do not lend themselves to elaborate protection schemes and self-diagnostics to a submodule level. A higher maintenance, repair and component costs are due to system complexity of analog systems. As a result of the present digital approach, there is savings in maintenance/repair and assembly costs due to integrated diagnostic functions. The encoded fault at the subassembly level is stored in a fault register for use by the serviceman. The fault is displayed (LED) for a short period of time (about 15-20 seconds) on command to facilitate the easy replacement of the damaged parts. It requires only 5 bits of memory to store as many as 31 faults and requires a 5 LED display.

2.4.1 Fault Diagnostics

The reader is referred to Figures 1 and 2 to understand the operation of the fault diagnostics. Two important signals, VB and I, are utilized in the fault determination scheme. Although VB and I signals are oscillatory, only their peak values are of interest. The strobe generating circuit of the DPSC generates strobes at the middle of the on time of drive signals (Φ 1 and Φ 2). The DPSC strobes (monitors) VA1, VB1, I1 and Ip inputs giving them sufficient time to settle down before being strobed. It checks for specific combination of conditions to occur for a prescribed number of times successively to determine the catastrophic failure of certain elements in the power system. Some of the failure modes are monitored during the "power up sequence" and "regulation mode" while others during the later only. The fault conditions are the combination of voltage and current levels on these inputs. Elements in the power filter stage, such as diodes, inductor and capacitor are checked for failure modes as open or short. The faults are priority encoded to avoid chain reaction catastrophic failures. Highest priority is given to the most destructive fault. The detected and encoded fault condition is stored and displayed (LED's) on command providing easy serviceability.

For example, one such condition for fault recognition for shorted diodes (D1 and D2) could be:

FDS = (I1VH. VB1L .STB)FC1,

where I.VH indicates current level on I1 input very high, greater than the certain percent of its normal peak value. VB1L is the voltage level corresponding to the voltage at point B, being less than a preset percent of its normal value. STB is the appropriate strobe signal and FC1 is the number of successive times the condition should hold (in this case 1).

2.4.2 System Protection

The description of system protection functions is as follows:

(i) Output Over Voltage: When the voltage level at point A rises above the predetermined threshold value and stays there for a certain period of time to avoid nuisance tripping, the over voltage fault is detected, encoded and stored. This fault condition is displayed (LED) and switching inhibited. This condition is not strobed but continuously monitored.

(ii) Secondary Circuit Over Current: When the inductor current rises above the predetermined current level, the DPSC outputs (forces) the minimum pulse width so long as that condition exists and then goes to a normal operating mode.

(iii) Primary Overcurrent: When the detected current, Ip, at the primary side of the transformer rises above the predetermined threshold, the fault is detected, encoded and stored. The fault condition is displayed (LED) and switching signals (drive signals) are inhibited. This signal is continuously monitored and not strobed because of the severity of its effects and damages.

3.0 RESULTS

An actual breadboard prototype using CMOS/TTL logic was constructed and various tests were performed on a 5 V, 12 A, double ended, half bridge power supply. Although the breadboard contained diagnostic and system protection functions, only the regulation performance is described here. The following is an example of the regulation performance. Refer to Figure 5.

	Dynamic Load Change	
	12A to 6 A	6A to 12 A
Initial Excursion =	500 mV	50 mV
Recovery Time =	800 us	600 us
Static Error =	~0	~0

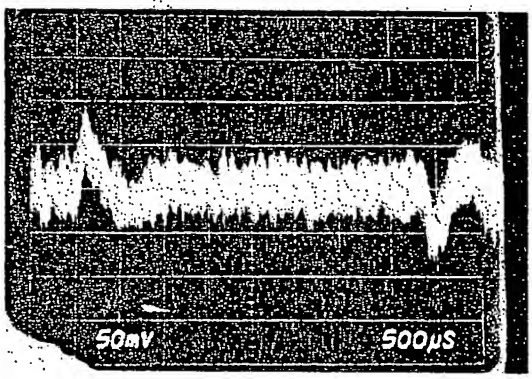


Figure 6 - Dynamic Load Effect

Results of with and without the anticipatory control are depicted below for line changes from 104 VAC to 127 VAC for minimum (20%) and maximum (100%) load conditions.

(i) Without compensation control

	Output Voltage VA With	
AC Line Voltage	Min. Load 2.4 A	Max. Load 12 A
104 VAC 115 VAC 127 VAC	5.047 V 5.065 V 5.081 V	5.032 V 5.049 V 5.066 V
Change in output voltage	Δ VA = 34 mV	Δ VA = 34 mV

Total load/line regulation:
VA = 49 mV (~ 1%)

(ii) With compensation (control)

AC Line Voltage	Output Voltage VA With Min. Load 2.4 A	Output Voltage VA With Max. Load 12 A
104 VAC	5.017 V	5.008 V
115 VAC	5.018 V	5.006 V
127 VAC	5.016 V	5.004 V
Change in output voltage	VA = 1 mA	ΔVA = 4 mV

Total load/line regulation:
VA = 14 mV ($\sim$ 0.3%)

4.0 CONCLUSION

Using microcontroller system feedback and control, an optimal, versatile digital power system controller with features outlined can be developed into a single LSI chip. The results of the breadboard evaluation has identified that excellent line and load regulation which competes with present analog systems can be accomplished. Through programmability, it offers flexibility and adaptabilility to different designs. The fault diagnostic features is the "kohinoor" of the crown not found in the analog systems. It offers easy serviceability and maintainability of the power systems. A multilevel power supply could be regulated using the same controller by multiplexing the outputs.

As of the writing of this paper, NCR is entering into a custom LSI design phase of the DPSC concept. The LSI chip, which contains all the sequencing, regulation, system protection, and fault isolation diagnostic functions, as described, is being implemented in NMOS technology to support up to a triple output power system.